CLAIMS

1. An apparatus comprising:

a circuit configured to (i) monitor a plurality of signals for transitions and (ii) invert said signals when at least a predetermined number of said signals transition in a predetermined direction; and

a plurality of buffers configured to present said signals received from said circuit on a transmission bus.

2. The apparatus according to claim 1, wherein said circuit is further configured to invert said signals when at least said predetermined number of said signals transition in an opposite direction of said predetermined direction.

3. The apparatus according to claim 1, wherein said predetermined number is greater than one half of a total number of said signals.

4. The apparatus according to claim 1, wherein said circuit comprises:

a transition checker circuit configured to present a plurality of transition signals each indicating a transition direction of one of said signals;

a control circuit configured to present a flag signal when at least said predetermined number of said transition signals have said predetermined direction; and

an inverter circuit configured to invert said signals in response to said flag signal.

5. The apparatus according to claim 4, wherein said buffers are further configured to present said flag signal on said transmission bus.

6. The apparatus according to claim 4, wherein said transition checker circuit comprises:

a plurality of flip-flops configured to present said signals as a plurality of sampled signals;

a plurality of inverters configured to present said signals as a plurality of inverted signals; and

a plurality of logic gates configured to present said transition signals in response to said sampled signals and said inverted signals.

7. The apparatus according to claim 4, wherein said circuit further comprises a plurality of flip-flops configured to store said signals as presented by said inverter circuit.

8. The apparatus according to claim 7, wherein said circuit further comprises a clock configured to present a clock signal to said flip-flops.

9. The apparatus according to claim 8, wherein said buffers are further configured to present said flag signal on said transmission bus and said transition checker circuit comprises:

a plurality of flip-flops configured to present said signals as a plurality of sampled signals;

a plurality of inverters configured to present said signals as a plurality of inverted signals; and

a plurality of logical gates configured to present said transition signals in response to said sampled signals and said inverted signals.

10. A method of reducing noise induced by transitions of a plurality of signals, the method comprising the steps of:

(A) monitoring said signals for said transitions;

(B) inverting said signals in response to at least a predetermined number of said signals transitioning in a predetermined direction; and

(C) presenting said signals on a transmission bus.

11. The method according to claim 10, further comprising the step of inverting said signals in response to at least said predetermined number of said signals transitioning in an opposite direction as said predetermined direction.

12. The method according to claim 10, wherein said predetermined number is greater than one half of a total number of said signals.

13. The method according to claim 10, wherein step (A) comprises the sub-steps of:

generating a plurality of transition signals each indicating a transition direction of one of said signals; and

generating a flag signal when at least said predetermined number of said transition signals have said predetermined direction.

14. The method according to claim 13, further comprising the step of presenting said flag signal on said transmission bus.

15. The method according to claim 13, wherein presenting said plurality of transition signals comprises the sub-steps of:

sampling said signals to present a plurality of sampled signals;

inverting said signals to present a plurality of inverted signals; and

logically combining said sampled signals and said inverted signals to present said transition signals.

16. The method according to claim 13, further comprising the step of storing said signals prior to presenting said signal on said transmission bus.

17. The method according to claim 16, further comprising the step of generating a clock signal to control said storing.

18. An integrated circuit comprising:

means for monitoring a plurality of signals for transitions;

means for inverting said signals in response to at least a predetermined number of said signals transitioning in a predetermined direction; and

means for presenting said signals on a transmission bus.